Semi-high technology Inc.

Lens AutoFocus Driver   Preliminary   SM9714

FEATURES

- VCM driver for auto-focus
- 10 bit resolution current sinking of 120mA for VCM
- VCM slew rate control (SRC) – Linear slope control,Dual level control
- Supply voltage range (VDD) : 2.3V to 3.6V
- Fast mode I2C interface (1.8V interface available)
- Power on reset (POR)

- Package : 0.82mm(W) * 1.32mm(H) *0.3mm(T)
- 6pins WLCSP

APPLICATIONS

- Cell Phone Auto Focus
- Web and PC cameras
- Security cameras
- Image stabilization

DESCRIPTION

The SM9714 is single 10-bit DAC with 120mA output current sink capability. Designed for linear control of voice coil motors, the SM9714 is capable of operating voltage to 3.6V. The DAC is controlled via a I2C serialinterface that operates DAC by clock rates up to 400kHz.The SM9714 incorporates with a power-on reset circuit, power-down function, and exactly matched sense resistor. Power-on reset circuit ensure when supply power up, DAC output is to 0V until valid write-bit value takes place. It has a power down features that reduces the current consumption of the device to 1uA maximum. The SM9714 is designed for auto focus and optical zoom camera phones, digital still cameras, and camcorders applications. The I2C address for the SM9714 is 0x18.

FUNCTIONAL BLOCK DIAGRAM
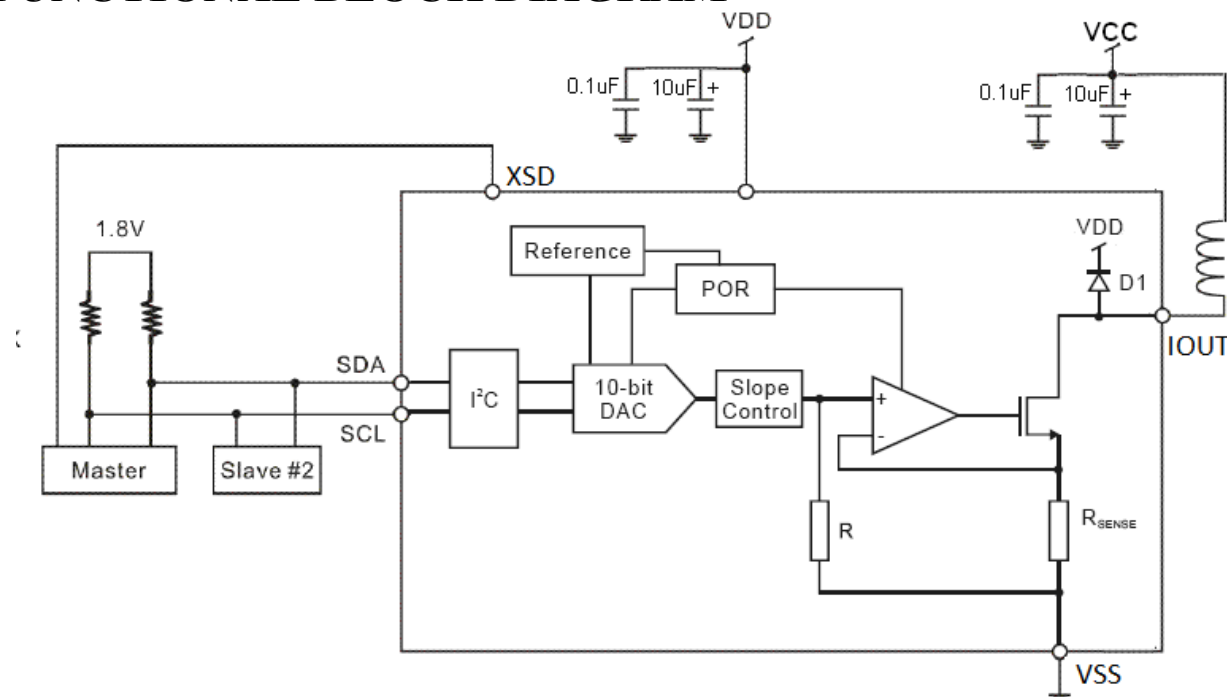
PIN CONFIGURATION AND PIN DESCRIPTION

WCSP-6

Top View   Bottom View
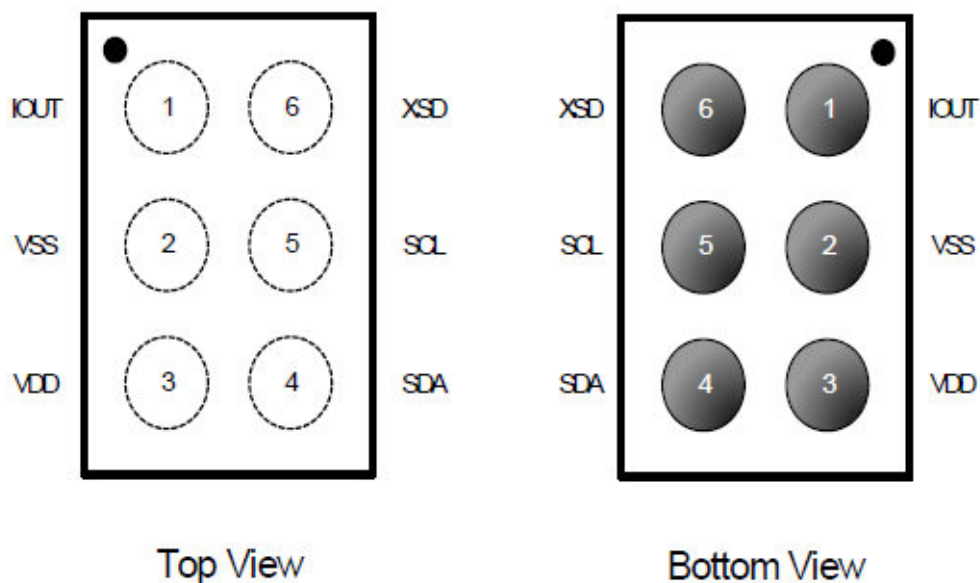
IC size : 0.81(W) X 1.31(L) X 0.30(T) (mm)
Minimum pin pitch = 0.4mm (6pins WLCSP)

PIN DESCRIPTION

No.	Pin name	I/O	Description
1	IOUT	O	Output current sink
2	VSS	-	Ground
3	VDD	-	Power supply
4	SDA	I/O	I2C interface input (DATA)
5	SCL	I	I2C interface input/output (CLOCK)
6	XSD(1)	I	Shutdown mode (active low)

(1) XSD : Shutdown mode (active low)
1: Normal operation

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, Ta=25℃)

Symbol	Parameter	Min	Max	Unit
VBB_{DDBB}	VDD to GND	-0.3	4.5	V
Vin	Control input voltage	-0.3	VDD+ 0.3	V
Vhbm	Human body model		2	KV
Vmm	Machine model		200	V
IBB_{SINKBB}	ISINK to GND		$-0.3 \sim V_{DD}+0.3$	V
Topr	Operating temperature	-45	-40 ~ +85	℃
Tstg	Storage temperature		-65 ~ +150	℃
Tjmax	Junction temperature		150	℃

Note> Continuous Power Dissipation (Ta=25℃)
0.82mm X 1.32mm WLCSP, 100 ℃/W

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range(Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode when the absolute maximum ratings may be exceeded is anticipated.

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	unit
VDD	Power supply voltage	2.3	2.8	3.6	V
Vin	Control input voltage	1.8	2.8	VDD	V
SCL	I2C bus transmission rate			400	K HZ

Note:
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VDD=2.3 to 3.6V, Vin=1.8V to VDD, Ta= -40 to 85℃, unless otherwise specified. Typical values are at 25℃)

| Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DC Performance						
Supply Voltage	VDD		2.3		3.6	V
VDD Current	I_{SD}	Shutdown mode	-1		+1	uA
	I_{PD}	Power down mode	-1	-	+1	uA
	I_Q	Quiescent mode	0.24	-	0.35	mA
Logic input / output (XSD)						
Input current			-1	-	+1	uA
Low Level Input Voltage	V_{IL}	-			0.54	V
High Level Input Voltage	V_{IH}	-	1.26			V
Logic input / output (SCL,SDA)						
Input current		-	-1		+1	uA
Low Level Input Voltage	V_{IL}	-			0.54	V
High Level Input Voltage	V_{IH}	-	1.26			V
Glitch rejection				50		nS
VCM driver						
Current resolution		117.3uA/LSB		10		bits
INL	INL		-4	-	+4	LSB
DNL	DNL		-1	-	+1	LSB
Zero code error	ZCE	Zero data loaded to DAC	-1	-	+1	mA
IOUT compliance voltage (1)		Output current = 100mA	150	-	-	mV
Maximum output current	Imax			120		mA
Power on time (2)	TPON			0.5		ms

(1) The output compliance voltage is guaranteed by design and characterization, not mass production test.
(2) SM9714 requires waiting time of 0.5ms after power on. During this waiting time, the offset calibration of internal amplifier is operating for minimization of output offset current .
(3) Maximum output current can be set 60mA to 140mA.

REGISTER
I2C FORMAT

■**Write operation**
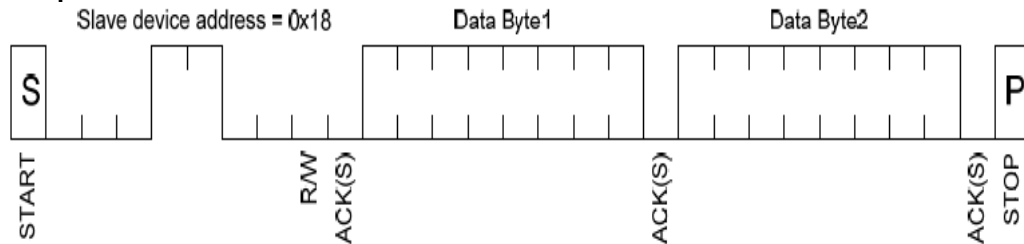
■**Read operation**

■
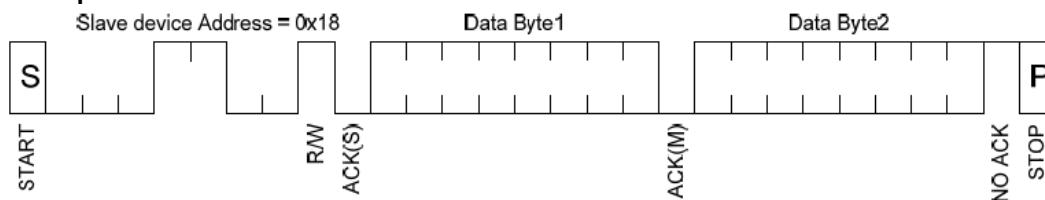
Register Format

Byte1								Byte2							
PD	FL AG	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S3	S2	S1	S0

PD : Power down mode
     1: Power down mode (active high)
     0: Normal operation mode

FLAG : FLAG must keep "L" at writing operation.

D[9:0] : Data input
     Output current = (D[9:0]/1023) X 120mA
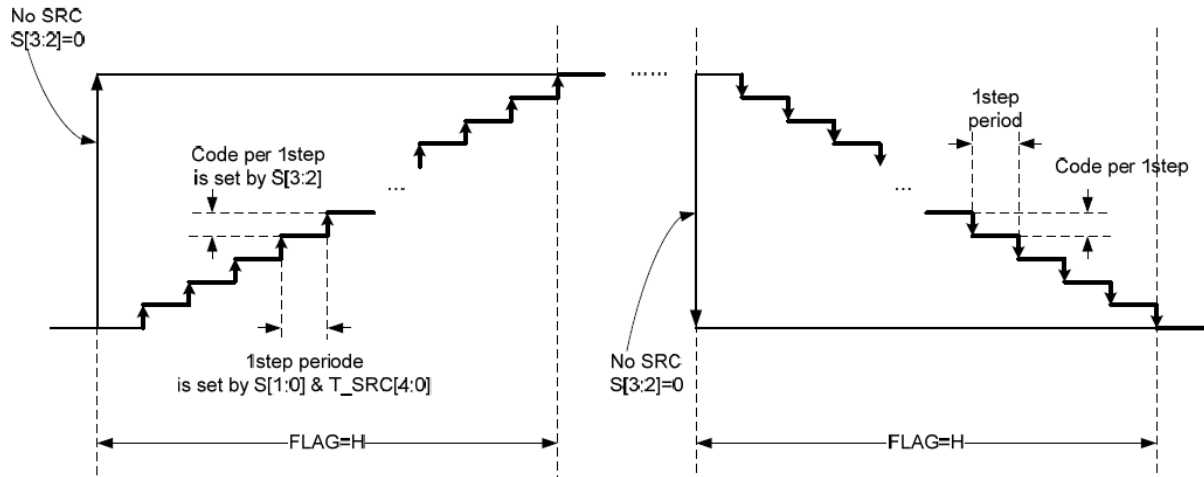   Max current = 120mA +/- 5%

S[3:2] : Codes per step

S[3:2]	Codes per step
0	0 (no SRC) – direct driving
1	1
2	2
3	4

S[1:0] : Step period

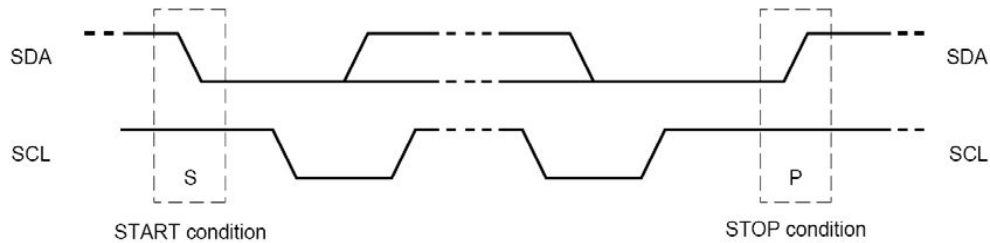| SRCT[1:0]	Period [us]
0	81
1	162
2	324
3	648

## SRC CONTROL SCHEME

SRC TEST RESULTS
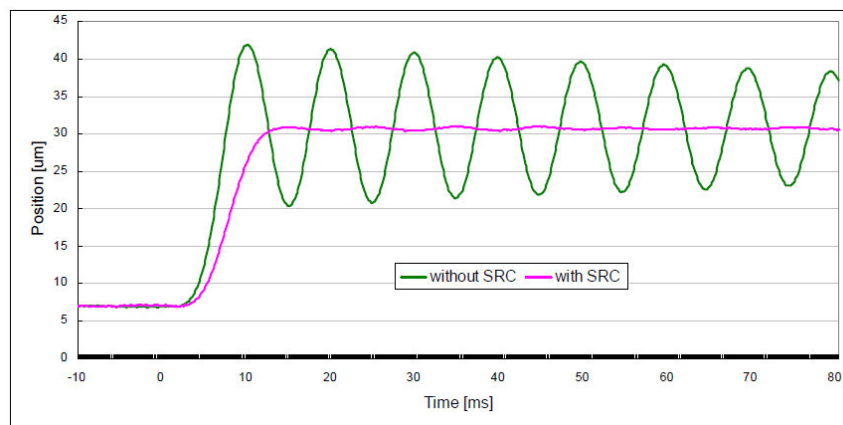
I2C PROTOCOL

■ **Start and Stop condition**

Within the procedure of the I2C-bus, unique situations arise which are defined as START (S) and STOP (P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

▪ **Complete I2C Data Transfer**
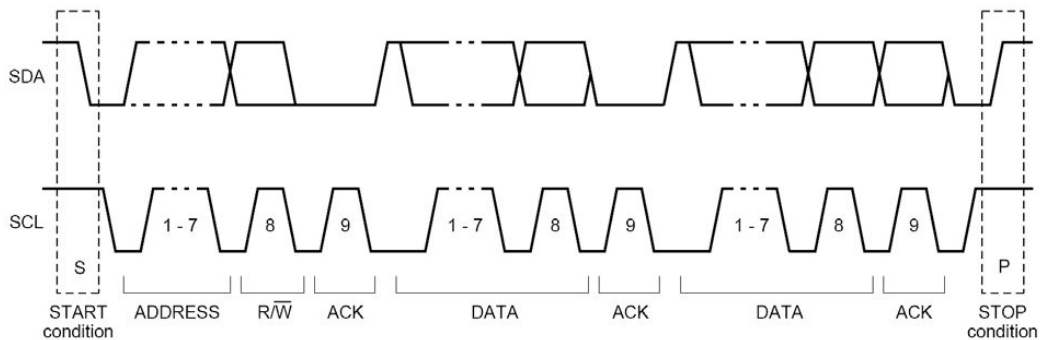
Data transfers follow the format. After the START condition (S), a slave address is sent. A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated

I2C TIMING

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition.	$t_{HD;STA}$	0.6	-	us
Low period of the SCL clock	t_{LOW}	1.3	-	us
High period of the SCL clock	t_{HIGH}	0.6	-	us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	us
Data hold time	$t_{HD;DAT}^{(1)}$	-	0.9	us
Data set-up time	$t_{SU;DAT}$	100	-	ns
Rise time of both SDA and SCL signals	t_r	$20+0.1C_b^{(2)}$	300	ns
Fall time of both SDA and SCL signals	t_f	$20+0.1C_b^{(2)}$	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	us
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	us
Capacitive load for each bus line	C_b	-	400	pF
Pulse width of spike suppress	t_{SP}	0	50	ns

(1) A master device must provide a hold time of at least 100ns for the SDA signal to bridge the undefined region of the falling edge of SCL. The maximum tHD;DAT has only to be met if the device does not stretch the LOW period (tLOW) of the SCL signal.
(2) Cb is the total capacitance of one bus line in pF, tr and tf are measured between 0.3VDD to 0.7VDD.
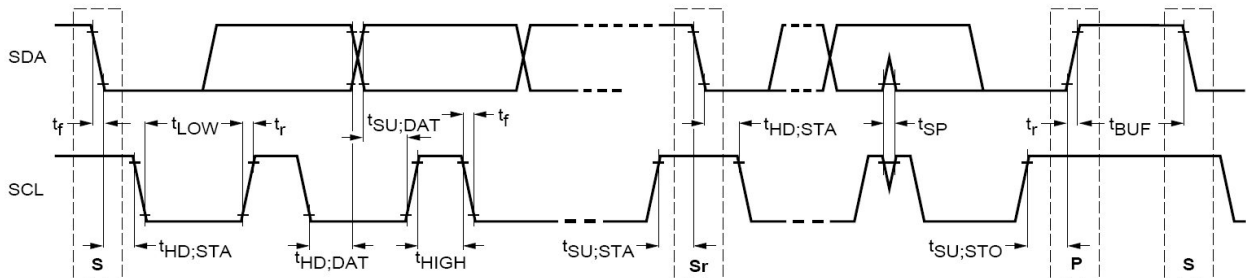
TYPICAL APPLICATION CIRCUIT
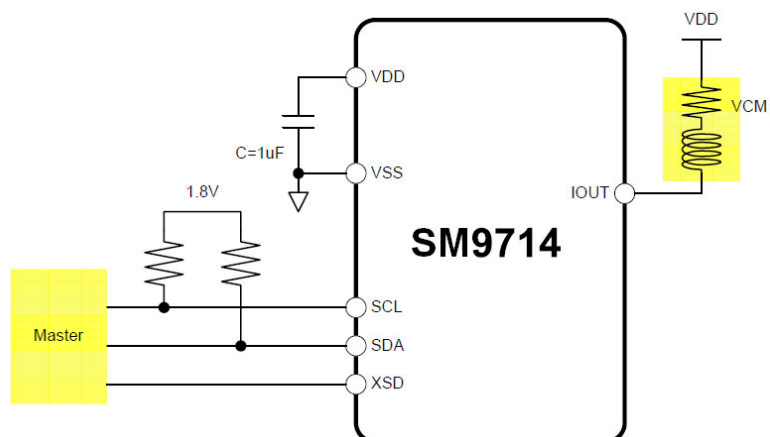
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
SM9714	6 Pins, WCSP	9714

PACKAGE DIMENSION (6 WLCSP 0.82 X 1.32 X 0.30)

* Unit : mm

WCSP-6

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.260	0.300	0.340
A1	0.065	0.080	0.095
A2	0.195	0.220	0.245
D	1.270	---	1.350
E	0.770	---	0.850
D1	0.750	0.800	0.850
E1	0.350	0.400	0.450
b	0.150	0.200	0.250
e	0.400 BSC		
SD	0.000 BSC		
SE	0.200 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		